EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	17684	@rlad<"20011016" and (test with (chip or IC) or PCB)	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/05 11:59
L5	4386	4 and interconnect$3	USPAT	OR	ON	2006/04/05 11:59
L6	1546	5 and (((resistor or resistive or resistance) and (capacitor or capacitance or capacitive)) or RC)	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/05 12:01
L7	1173	6 and ((input with output) or "i/o")	USPAT	OR	ON	2006/04/05 12:01
L8	993	7 and ((tun$3 or adjust$4 or vari$4) and (resistor or resistance or capacitor or capacitance))	USPAT	OR	ON	2006/04/05 12:02
L9	7	8 and (emulat$3 with interconnect$3)	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/05 12:30
L10	25	8 and ((emulat$3 or simulat$3 or imitat$3) with interconnect$3)	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/05 15:48
L11	20	8 and ((simulat$3 or imitat$3) with interconnect$3)	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:59
L12	3	09/728050	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/05 14:59
S1	2	09/951750	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2005/08/31 10:19
S2	64967	((resistor or resistive or resistance) and (capacitor or capacitance or capacitive)) and @rlad<"20011016"	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/05 12:00
S3	7733	S2 and interconnection	USPAT	OR	ON	2005/09/02 09:18

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S4	15096	S2 and interconnect$3	USPAT	OR	ON	2006/04/05 11:59
S5	12219	S4 and ((tun$3 or adjust$4 or vari$4) and (resistor or resistance or capacitor or capacitance))	USPAT	OR	ON	2006/04/05 12:01
S6	7874	S5 and ((input with output) or "i/o")	USPAT	OR	ON	2006/04/05 12:01
S7	2506	S6 and waveform	USPAT	OR	ON	2005/09/02 09:22
S9	1093	S7 and (PCB or (printed adj circuit or board))	USPAT	OR	ON	2005/09/02 09:23
S10	0	S9 and (RC adj ladder)	USPAT	OR	ON	2005/09/02 09:23
S11	354	S9 and RC	USPAT	OR	ON	2005/09/02 09:26
S12	0	2003/0050770a1	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2005/09/02 09:27
S13	0	0050770a1	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2005/09/02 09:27
S14	38	@rlad<"20011016" and (emulat$3 with interconnect$3 with (chip or pcb))	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/05 12:25
S15	7326	@rlad<"20011016" and (test with chip)	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/05 11:58
S16	252	@rlad<"20011016" and (test adj chip) and IC	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/04 15:17
S17	203	S16 and (interconnect$3)	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/04 14:15
S19	4	@rlad<"20011016" and (emulat$3 with interconnect$3 with (ic or pcb))	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2006/04/04 15:19